overdrive voltage V(ov)=(V(inp)-V(inn)) generate a differential current given by I(ov)=gm*V(ov), where gm is the transconductance of the input differential pair at the steady-state operating point V(ov)=0 volts (V); a gain stage node ngain converting the current I(ov) to (in the CMOS case) a voltage gain and having a transition speed depending on the overdrive current I(ov) available, the voltage excursion required between the high and low levels at the ngain node, and the capacitive load at the ngain node, including any Miller capacitance from the comparator's output stage; and a gain stage assuring a given slew rate at the comparator output out.

Please replace paragraph [0003] of the specification with the following:

Additional non-ideal effects for most comparators include random and systematic offset of the input differential pair, the common mode rejection ratio of the input differential pair, and power supply rejection and propagation delay dependence on the power supply voltage. For example, a comparator's propagation delay will typically be related to the applied overdrive voltage V(ov), with a lower overdrive voltage resulting in a longer propagation delay ~~(but consuming greater power)~~.

Please replace paragraph [0005] of the specification with the following:

There is, therefore, a need in the art for alternatives for reducing an integrated circuit comparator's propagation delay while ~~limiting~~ maintaining or reducing power consumption by the comparator.

Please replace paragraph [0006] of the specification with the following:

To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide, for use in an integrated circuit comparator, a pulsed rather than continuous bias current applied, in at least a fast comparator configuration, to a current source within a comparator's input gain stage. ~~driven by a current proportional to t~~The transconductance current will then~~of a differential pair of input transistors receiving voltage signals to~~ be ~~compared is~~ pulsed rather than continuous. The pulse width of the bias current is small relative to the system clock, but has a large current magnitude allowing the comparator to quickly respond to applied voltages. The end result is a fast comparator~~;~~ but without the large quiescent current associated with conventional fast comparators~~unacceptable increase in current and power consumption~~. A voltage limiter optimizes the ngain node voltage excursion.~~and~~ A built-in hysteresis circuit suppresses any spurious ~~currents when the~~

~~bias current pulse is inactive~~voltage spikes at the output node at every comparator's bias pusle. The bias current pulse and sampling of the comparator occur in predefined relation to the system clock.

Please replace paragraph [0024] of the specification with the following:

FIGURES 2A through 2C are timing diagrams illustrating operation of a low power integrated circuit comparator with fast propagation delay according to one embodiment of the present invention. FIGURE 2A illustrates operation of comparator 100 in the low power comparator configuration. When the applied overdrive voltage V(ov) changes from +10 milli-Volts (mV) to 0, the voltage at node ngain changes slowly and the output voltage does not change (i.e., remains at 3 V or a logical "high"). Once the applied overdrive voltage V(ov) changes to –10 mV, the output voltage out toggles (i.e., changes to ~~=1.~~0 V or a logical "low").

Please replace paragraph [0025] of the specification with the following:

At room temperature with an integrated circuit comparator fabricated with typical processes and a V(inn) of 1.5 V, the worst case propagation delay for an overdrive voltage V(ov) varying between ±10 mV, a worst case output propagation

delay is approximately 5 microseconds (μs). Moreover, the propagation delay increases if the overdrive voltage V(ov) decreases. If V(ov)=±3 mV, the propagation delay increases to 30 μs. Comparator 100 will not toggle in the low power comparator configuration for (ov)<2.5 mV.

Please replace paragraph [0032] of the specification with the following:

FIGURE 3 is a block diagram of a low power integrated circuit pulse generator and comparator according to one embodiment of the present invention. System 300 includes pulse generator 301, a buffer or inverter 302, and comparator 100. The circuit 300 receives as inputs power supply voltages vss and vdd, a reference voltage vref and an input signal in to be compared to the reference voltage, an enable input enable, a phase triggered clock signal phase, a bulk bias voltage nbulk, comparator bias current icomp and a signal ibiaspulse biasing the pulse generator block and selecting pulsed biasing of the comparator 100.

Please replace the Abstract on page 24 of the specification with the following:

A direct relationship exists between an integrated comparator's propagation delay and the input differential pair's bias current and overdrive voltage. A new

method using a pulsed bias scheme for the input differential pair improves propagation delay by more than one order of magnitude without increasing significantly the average quiescent current, as long as the pulse width of the bias current is small relative to the system clock. ~~In at least a fast comparator configuration, the bias current applied to a current source within a comparator's input gain stage driven by a current proportional to the transconductance of a differential pair of input transistors receiving voltage signals to be compared is pulsed rather than continuous. The pulse with of the bias current is small relative to the system clock, but has a large current magnitude allowing the comparator to quickly respond to applied voltages, but without unacceptable increase in current and power consumption.~~ A voltage limiter optimizes the comparator's transition time and a built-in hysteresis circuit minimizes spurious ~~currents~~output transitions whenever the pulsed bias current pulse ~~is inactive~~changes state. The bias current pulse and sampling of the comparator occur in predefined relation to the system clock.